Influence of Process Conditions on Structural and Electrical Properties of $Hf_{1-x}Zr_xO_2$: Dead Layer Effect and Defect Trapping

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The recently discovered ferroelectricity in doped hafnium oxide was explained by stabilization of an orthorhombic phase [1]. Of all dopants an equal solution of hafnia and zirconia ($Hf_{0.5}Zr_{0.5}O_2$) showed the widest process window [2]. However the ferroelectric and dielectric properties strongly depend on the detailed processing conditions [3].

Planar metal-ferroelectric-metal (MFM) stacks of different composition and thickness were prepared by atomic layer deposition for the $Hf_{1-x}Zr_xO_2$ films and reactive physical vapor deposition for the TiN electrodes. The capacitor structures were annealed slightly above crystallization temperature (450°C) in N_2-atmosphere. Film thickness, annealing temperature, purge time in between ALD-pulses and Hf/Zr-ratio were varied and the influence analyzed by impedance spectroscopy, grazing-incidence X-ray diffraction (GIXRD), dielectric relaxation spectroscopy (DR) and scanning (SEM) and transmission electron microscopy (TEM). Additionally, polarization- and capacitance-voltage curves were measured during electric field cycling.

Crystallization is initialized during an annealing step at temperatures above 450°C. Due to the small film thickness of around 10 nm the grain size is limited to few nanometers (Fig. 1). The grain size is expected to have a strong influence on the coercive field. In addition, a non-switching dielectric layer at the interface is proclaimed which influences the switching behavior and the switching fields. Impedance spectroscopy revealed a strong influence of the processing conditions on the interfacial layer between electrodes and ferroelectric film. With increasing annealing temperature and purge times the dielectric interfacial layer capacitance C_{IF} decreased (Fig 2). This so called dead layer strongly influences the ferroelectric properties such as the coercive field and remanent polarization. In addition, dielectric relaxation which is reported to be connected to defects is strongly affected. These defects are suspected to be the root cause of wake up phenomenon [2]. Adjusting and understanding this interface is therefore crucial to reach outstanding performance.

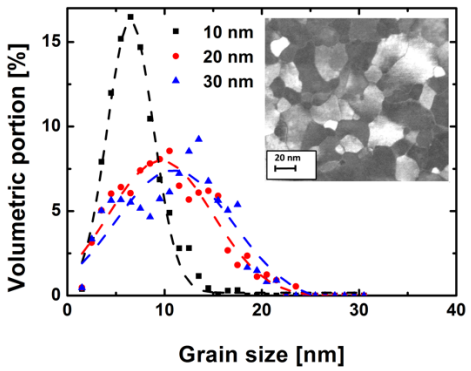

Figure 1. Top down TEM image of a ~10 nm thick $Hf_{1-x}Zr_xO_2$ layer (inset). Analysis of the grain radius results in Poisson distributions shown for 10, 20 and 30 nm thick films.

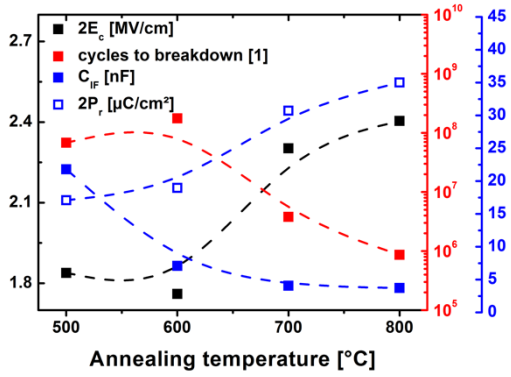

Figure 2. Comparison of E_C, breakdown stability, interfacial dead layer capacitance and remanent polarization P_r as a function of anneal temperature.

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[3] M. H. Park et al. *ACS applied materials & interfaces* (2016).
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